PyAEDT 驅動的PDN模擬自動化：從想法到實現

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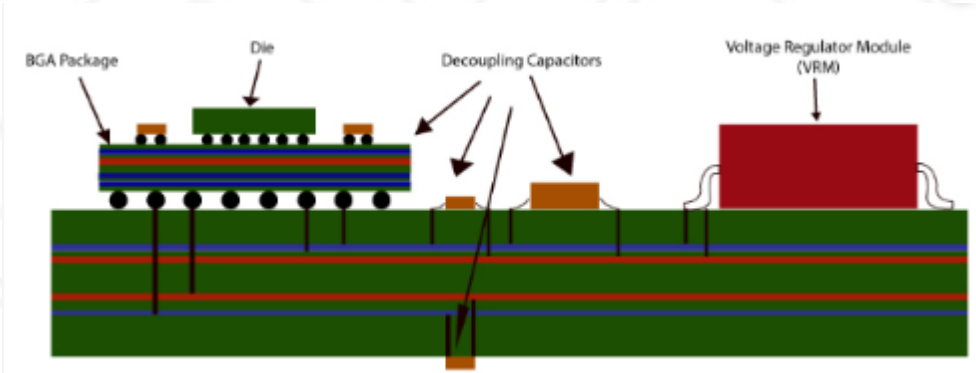
Agenda

- Motivation & Purpose
- PyAEDT = Python + AEDT
- Auto-Sim：PDN “All-In-One”
- More Feature
- Streamlit + PyAEDT
- Conclusion
- Reference

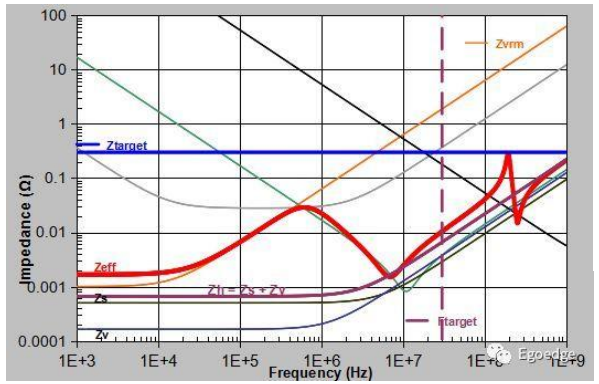
Motivation & Purpose

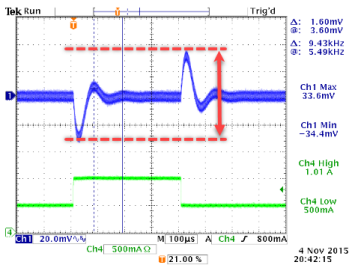
Why we talk about PDN ?

- There are some issues with insufficient transient margin during the VRTT test on different new platform
  - Transient margin can be improved by ***optimizing PDN***
- Perform PDN simulation quickly and accurately to meet the high demand for these requests.



$$V_{ripple}(f,t) = I_{transient}(f,t)Z(f)$$





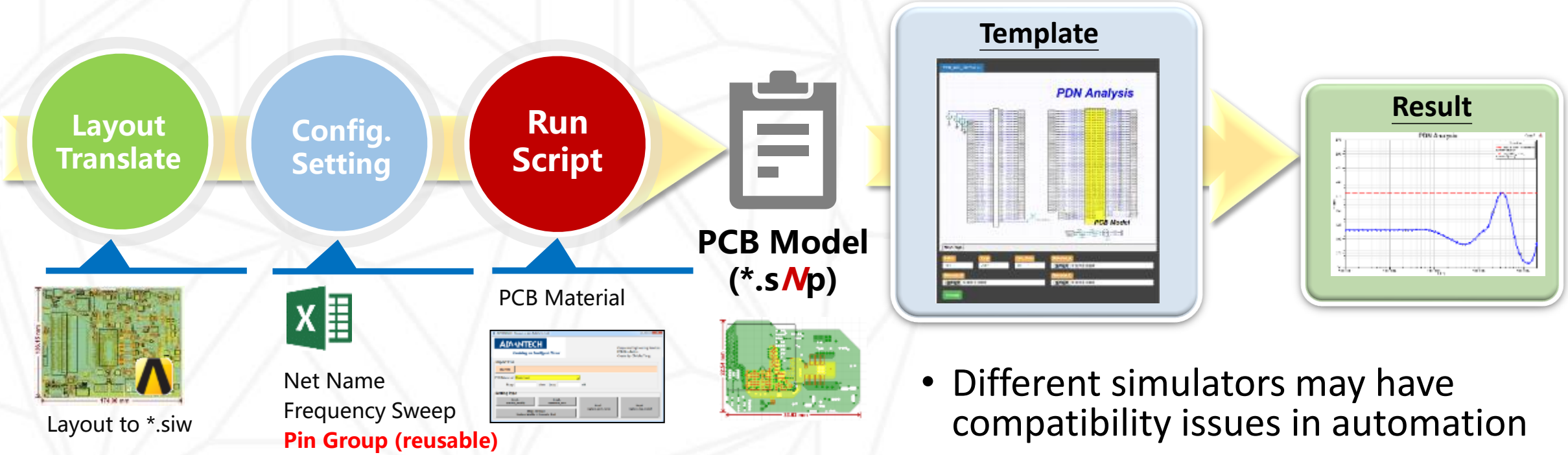
Motivation & Purpose
The Necessity of Automation

- Challenges and limitations of manual simulation
  - Avoid setting mistakes
  - Consistency
- Benefits of auto-simulation
  - More time to do root cause analysis
- PDN simulation “ALL in ONE” !!
  - Only one button clicking
  - Fully Auto-simlution

Auto-Sim
Further Evolution!!

Motivation & Purpose

Past : Semi-automation



- Some tasks are performed by human operators
  - More susceptible to human error
  - Less efficient than fully automation

- Different simulators may have compatibility issues in automation

Purpose

Now : All-In-One Automation

Upload board file ONLY

PyAEDT = Python + AEDT

Why PyAEDT ?

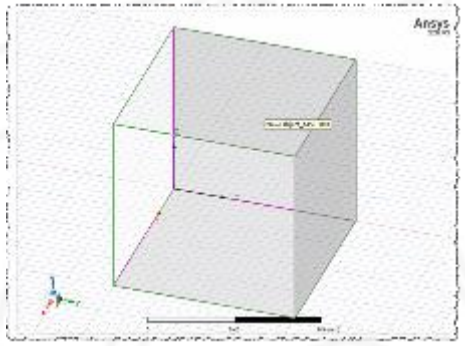
PyAEDT

```
hfss.modeler.create_box([0,0,0],[10,10,10])
```

Classical API

```
oEditor.CreateBox(
        [
            "NAME:BoxParameters",
            "XPosition:"      , "0mm",
            "YPosition:"      , "0mm",
            "ZPosition:"      , "0mm",
            "XSize:"          , "1mm",
            "YSize:"          , "1mm",
            "ZSize:"          , "1mm"
        ],

        [
            "NAME:Attributes",
            "Name:"           , "Box1",
            "Flags:"          , "",
            "Color:"          , "(143 175 143)",
            "Transparency:"   , 0,
            "PartCoordinateSystem:", "Global",
            "UDMId:"          , "",
            "MaterialValue:"  , "\"vacuum\"",
            "SurfaceMaterialValue:", "\"\"",
            "SolveInside:"    , True,
            "IsMaterialEditable:" , True,
            "ShellElement:"   , False,
            "ShellElementThickness:", "0mm",
            "IsMaterialEditable:" , True,
            "UseMaterialAppearance:", False,
            "IsLightweight:"  , False
        ])
```



- Recorded code is dirty and difficult
- Recorded scripts are difficult to reuse and adapt.

PyAEDT Provide:

- **HFSS & HFSS 3D Layout**
- **EDB**
- **Nexxim (Designer)**
- Twin Builder
- Mechanical
- Icepak
- Maxwell 2D, Maxwell 3D, RMXprt
- 2D Extractor & Q3D Extractor

PyAEDT = Python + AEDT

Stackup

- ✓ Thickness
- ✓ Material Library
- ✓ Roughness
- ✓ Trace Cross-Section

Option and Setting

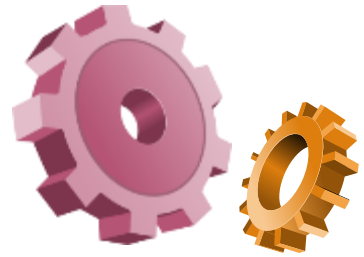
- ✓ Frequency
- ✓ Cut-out
- ✓ Sweep Selection

Comp. Model

- ✓ Capacitor, CMF…etc.

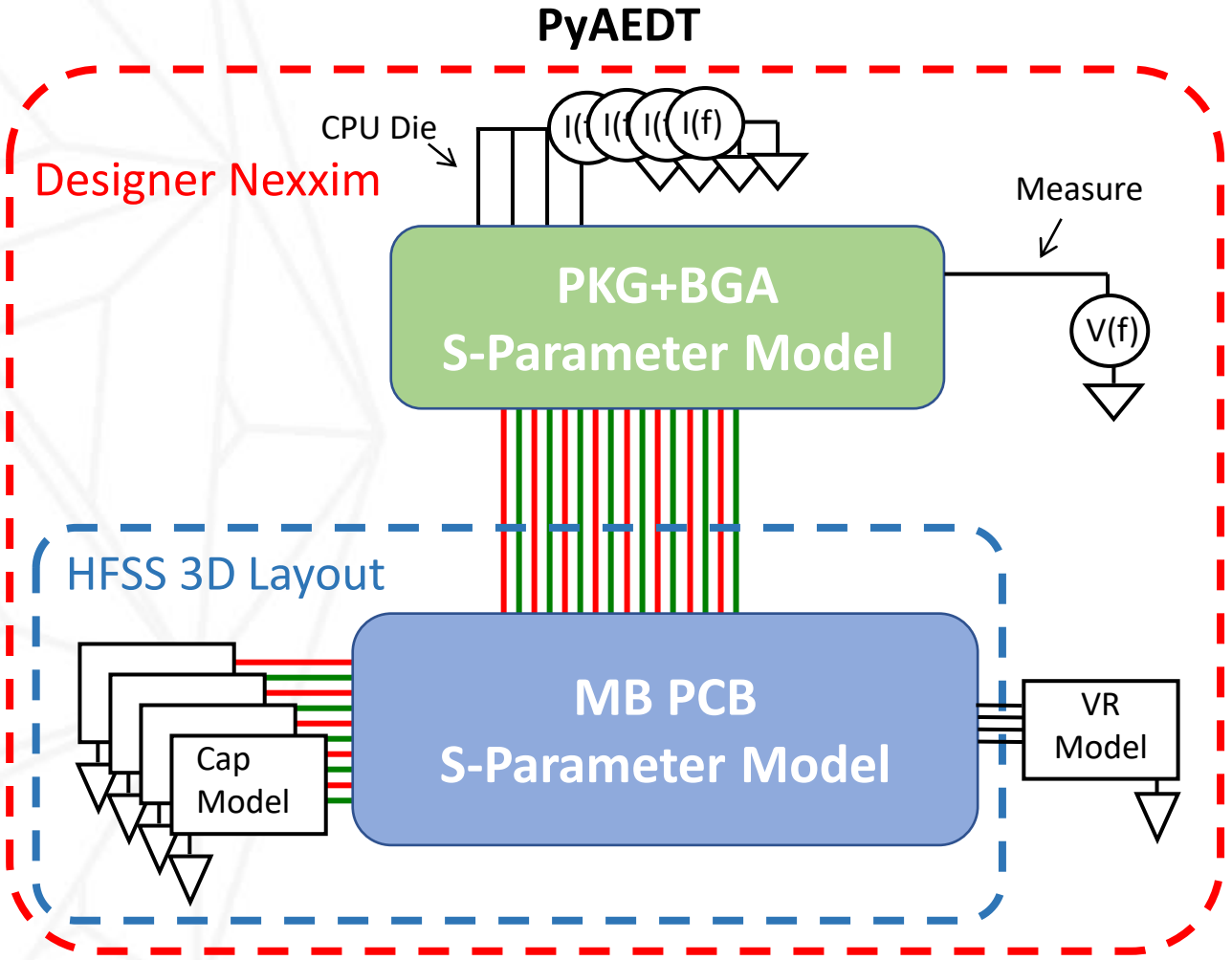
Pin Group & Port

- ✓ Signal/PWR, port
- ✓ Pin Group



Auto-Sim：PDN “All-In-One”

- **Now only 20 minutes** to run a case
  - 4-6 hours before
- PDN simulation workflow :
  - Extract PCB S-parameter
  - Run circuit simulation
- Using PyAEDT to integrate HFSS3D Layout & Designer

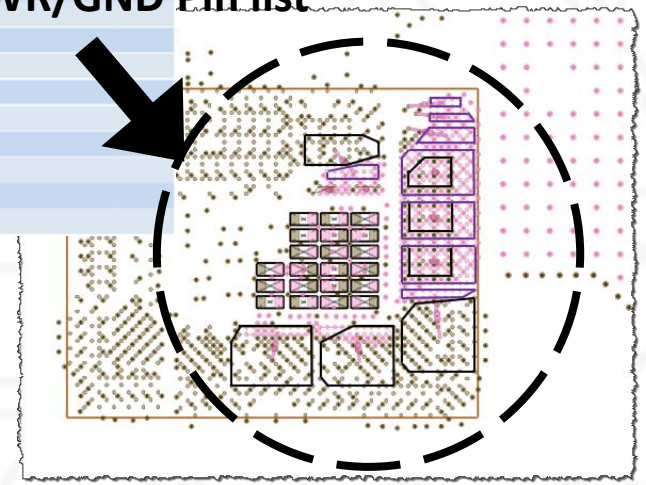


Auto-Sim：PDN “All-In-One”

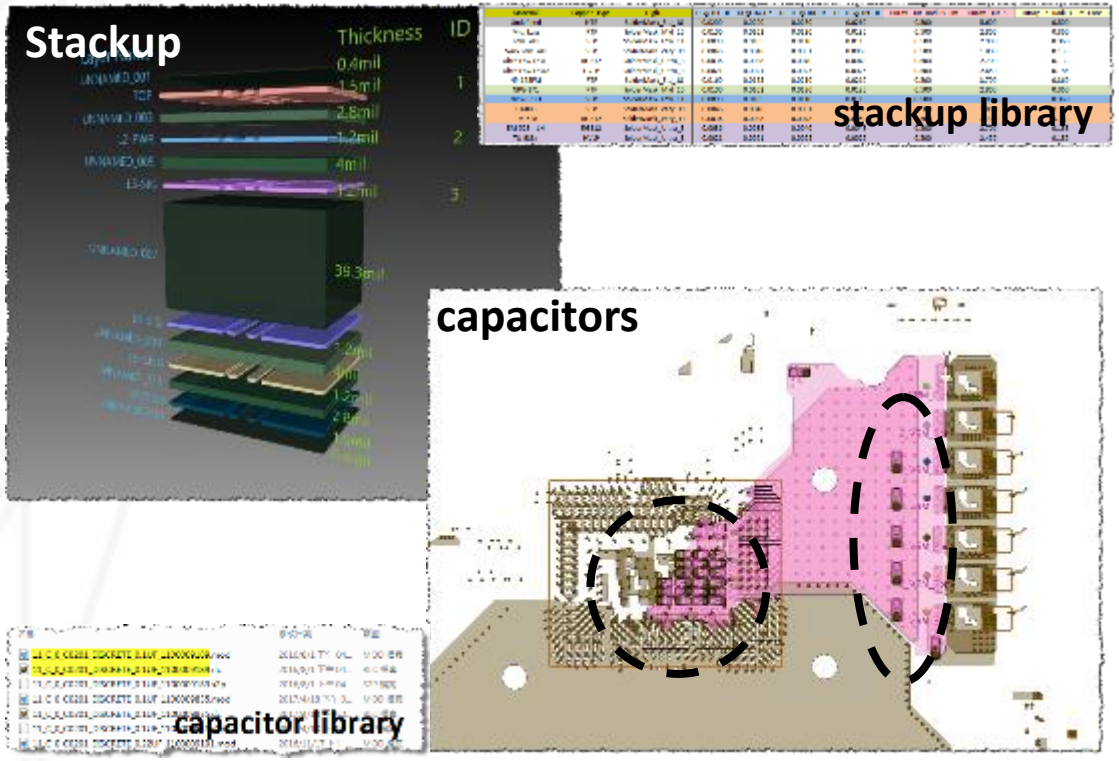
Auto-create pin group & port

Port#	PWR BGA Pin List	GND BGA Pin List
Port1	A20, B20, C20, D20	B21, C21, D21
Port2	F20, G20, H20, J20	F21, G21, H21, J21
Port3	A18, A17, A15, B17, C17, C18, C15	B18, B15
Port4	D18, D17, D15, F17, G18. G17, G15	F18, F15
Port5	D11, D14, D12, F14, G14, G11, G12, F11	F12, E9, D9
Port6	A14, B14, C14, A11, A12, C11, C12, B11	B12, B9, C9
Port7	H18, H17, H15, J17	J18, J15
Port8	H11, H14, H12, J14, J11, K11	J12, J10
Port9	A8, B8, C8, C7, D7	B7, D6
Port10	J8, J7, H8, H7, H6, H5	J6, J5, G9
Port11	C3, B3, C2	A3, B2, C1
Port12	F8, F7, F6, F5, E4, D4	F4, D8, D5
Port13	B6, C6, A6, A5, B4	B5, A4, C4
Port14	L10, M9, L8, L7	K9, L6
Port15	T9, U10, U8, V9, W8, W9	U7, W7, W10
Port16	N8, P8, T8, N7	N6, P7, T7
Port17	N9, R9, T10, N10	P10
Port18	K2	K3

PWR/GND Pin list

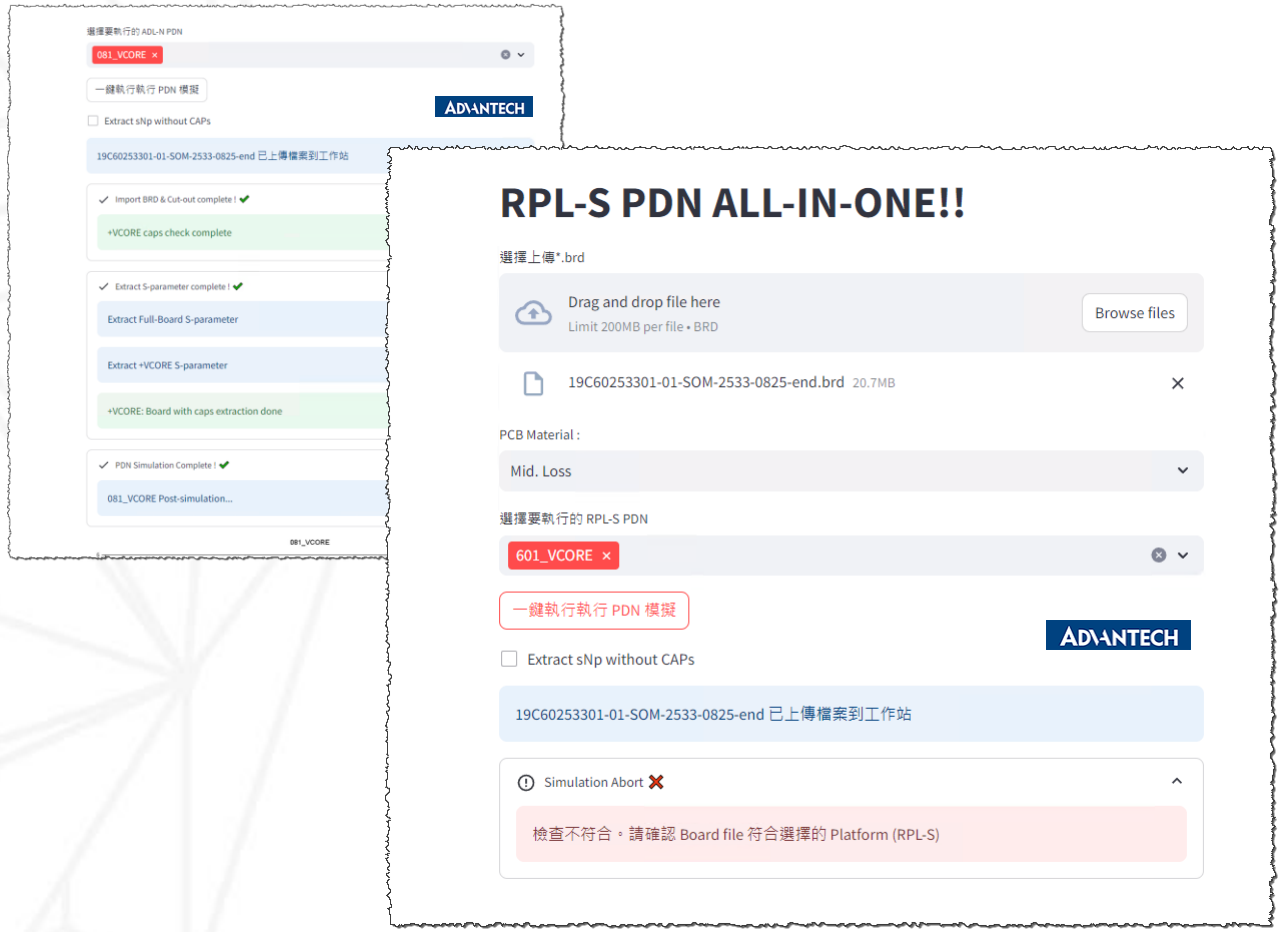


Auto-set stackup & cap model



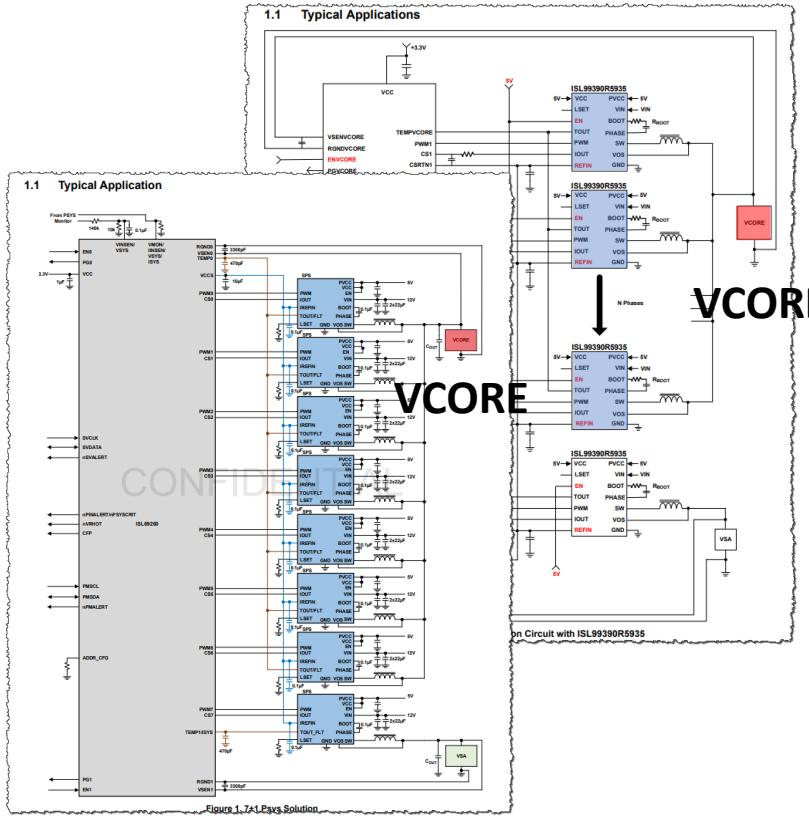
Auto-Sim：PDN “All-In-One”

- Error proofing :
  - Platform selection check
  - Capacitor model check
  - DC-short check



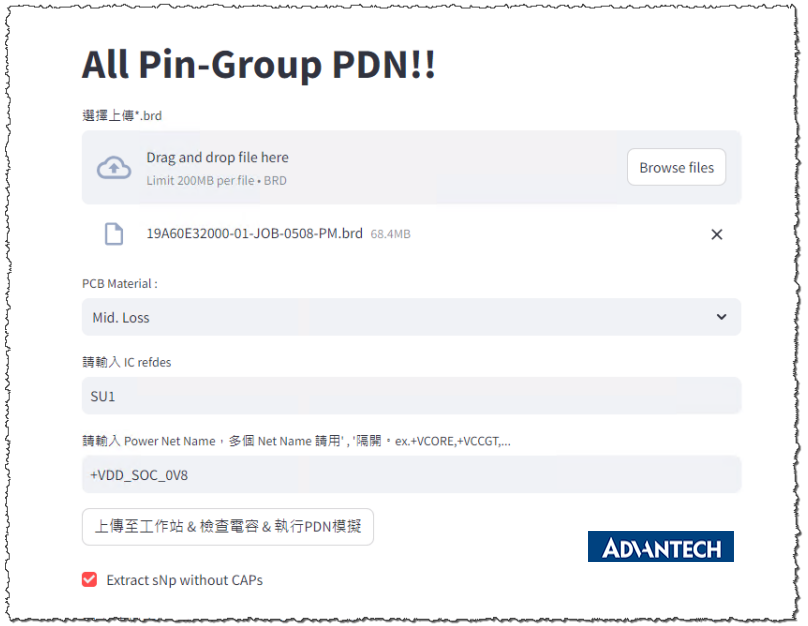
Auto-Sim：PDN “All-In-One”

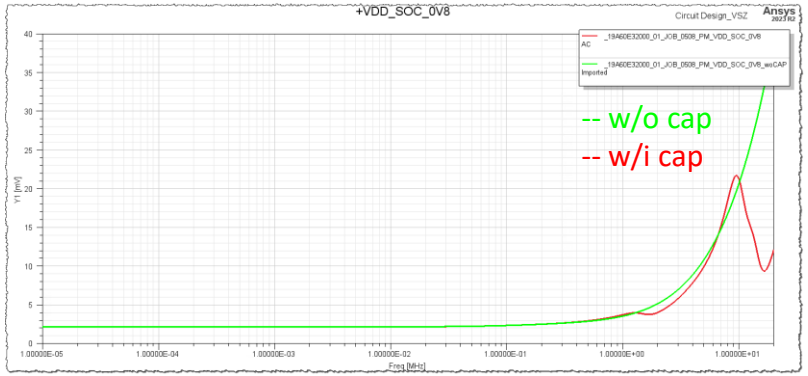
- The same platform may have different phases of VRM
  - VR model is described in netlist
- Using PyAEDT:
  - HFSS3dLayout :
    - Get the proper VRM port number
  - Designer :
    - Auto-modified the circuit netlist and run simulation



More Feature

- **Auto-Sim：“All-In-One”** additional option
  - Extract PCB s-parameter w/o cap
- PCB w/o cap gather more information
  - R_{dc} & $L_{parasitic}$ (power-ground loop)
- Another Feature :
  - Some platform do not specify pin list
    - All the identical power pin grouped together into a singe pin-group



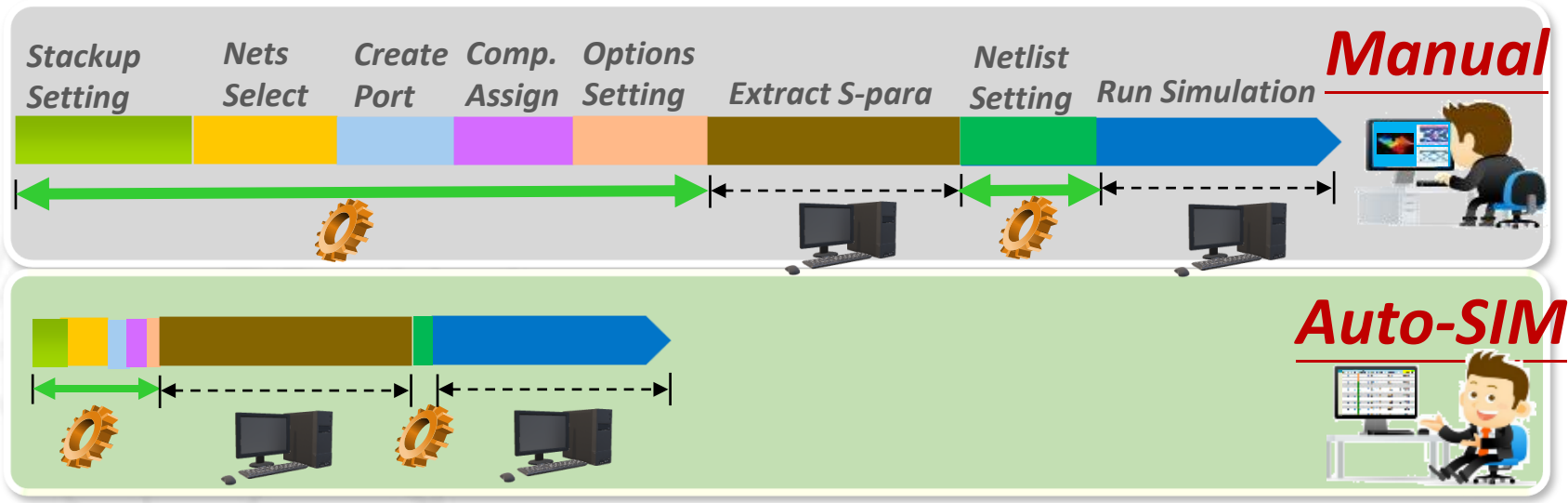


Streamlit + PyAEDT

- Open-source for web apps
- Python scripts to interactive UI
- Rapid deployment
- Data science friendly

Conclusion

- PyAEDT provide a user-friendly platform for SI engineers.
  - Enable automation and precise analysis
  - Requires no deep programming expertise
- Show how to simplifies PDN simulation significantly
  - Now it only takes **20 minutes**, compared to **4-6 hours** before.



Reference

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- https://lin-ming-chih.gitbook.io/aedt-scripting-1/dao-lun/api-yu-pyaedt-han-shi-feng-ge-bi-jiao

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